IN THE CLAIMS:

Please cancel claims 1, 2, 3, 13, 15 and 16 without prejudice or disclaimer of the subject matter set forth therein.

Please amend claims 4, 6, 9 and 10-12, and add new claims 20-22 as follows

1-3. (CANCELED)

4. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the plurality of passive elements includes passive elements of a plurality of specifications.

5. (ORIGINAL) The passive element chip according to Claim 4, wherein the specifications include a resistance value, a capacitance value, an inductance value, and a quality factor value.

6. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the plurality of passive elements is divided into a plurality of groups having mutually different specifications.

7. (ORIGINAL) The passive element chip according to Claim 6, wherein the plurality of groups includes a group of high-frequency specifications and a group of low-frequency specifications.

8. (ORIGINAL) The passive element chip according to Claim 6, wherein the groups include a group composed only of inductors, a group composed only of capacitors, or a group composed only of resistors.

9. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the plurality of passive elements includes only passive elements of high-frequency specifications or only passive elements of low-frequency specifications.

10. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the plurality of passive elements is composed only of inductors or capacitors.

11. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the passive elements are inductors formed of the metal wires spirally disposed.

12. (AMENDED) The passive element chip according to Claim ~~1~~ 20, wherein the passive elements are capacitors in which the metal wires constitute parallel plane electrodes.

13. (CANCELED)

14. (ORIGINAL) The passive element chip according to Claim 12, wherein the electrodes further have second electrodes electrically connected to the first electrodes, and

the second electrodes are covered with a resin layer expect for a part thereof.

15 and 16. (CANCELED)

17. (WITHDRAWN) A manufacturing method for a passive element chip having a plurality of passive elements, comprising:

a step for processing an insulating layer and metal wires and depositing them on a substrate to form a plurality of passive elements;

a step for forming, on the insulating layer, a plurality of first electrodes to be connected to the plurality of passive elements; and

a step for covering the insulating layer with a protective film such that the plurality of first electrodes is exposed.

18. (WITHDRAWN) The manufacturing method for a passive element chip according to Claim 17, further comprising:

a step for covering the protective film with a photosensitive resin film such that the plurality of first electrodes is exposed;

a step for forming, on the photosensitive resin film, metal wires to be electrically connected to the plurality of first electrodes;

a step for forming second electrodes to be electrically connected to the metal

wires; and

a step for covering the metal wires and the photosensitive resin film with a resin layer such that the second electrodes are partly exposed.

19. (WITHDRAWN) A manufacturing method for a highly integrated module having a plurality of insulating layers, comprising:

a step for disposing a passive element chip, which includes a substrate, a plurality of passive elements formed on the substrate by first metal wires, and electrodes for electrically connecting the plurality of passive elements to an external source, on a surface of one of the plurality of insulating layers;

a step for disposing an active element chip, which has active elements and electrodes for electrically connecting the active elements to an external source, on a surface of one of the plurality of insulating layers; and

a step for electrically connecting the electrodes of the passive element chip and the electrodes of the active element chip by second metal wires.

20. (NEW) A passive element chip comprising:

a substrate;

an insulating layer formed on the substrate;

an inductor formed in the insulating layer by a first metal wire;

a capacitor formed in the insulating layer by a second metal wire, wherein the capacitor is isolated from the inductor;

a protective film formed on the insulating layer, wherein the protective film has a first opening for exposing the inductor and a second opening for exposing the capacitor;

a first wiring pattern formed within the first opening; and

a second wiring pattern formed within the second opening.

21. (NEW) A passive element chip formed by being diced off from a wafer, comprising:

a substrate;

an insulating layer formed on the substrate;

an inductor formed in the insulating layer by a first metal wire;

a capacitor formed in the insulating layer by a second metal wire wherein the capacitor is isolated from the inductor;

a protective film formed on the insulating layer wherein the protective film has a first opening for exposing the inductor and a second opening for exposing the capacitor;

a first wiring pattern formed within the first opening for connecting to an external source; and

a second wiring pattern which is formed within the second opening for connecting to the other external source.

22. (NEW) A highly integrated module comprising:

a first substrate;

an insulating film formed on the first substrate;

a passive element chip within the insulating film and being formed on the first substrate, and

a semiconductor chip within the insulating film and being formed on the first substrate;

wherein the passive element chip comprises:

a second substrate different from the first substrate;

an insulating layer formed on the second substrate;

an inductor formed in the insulating layer by a first metal wire;

a capacitor formed in the insulating layer by a second metal wire, with the capacitor being isolated from the inductor; and

a protective film formed on the insulating layer.